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Notes from the dedicated hardware discussion of Monday, November 10. The next meeting will be held Thursday, November 13 at 1:30 P.M. in the Penthouse.

Steve

Present: Jim Steimel, Vince Pavlicek, Luciano Piccoli, Dehong Zhang, Stephen Wolbers, Rob Kutschke, Bob Webber, Brian Chase, Mark Bowden

Main Topics: Digital Signal Receiver (DSR) and Echotek alternatives

Echotek:

The "Echotek board" with the FIFO replaced with dual-port memory, a Tundra VME interface instead of the Cyprus interface, and a mechanism to allow easier programming of the FPGA (but not a new FPGA) has been verbally quoted to Mark. What we would like to see are the details of the architecture in this case and a timescale and estimated cost (see action items at the end).

DSR:

First we addressed the capability of the DSP to handle 47 kHz from 8 input channels. Brian thought that this was not too terribly difficult, given the capabilities of the DSP. It is in fact good to something over 1 MHz, depending on the tasks which one is proposing to use the DSP for. So this does not seem to be a big issue.

Next we discussed the possiblity of bringing in timing signals to the DDC's. This looks to be a slight change to the board, primarily adding some traces to the board and some connectors on the front. A board could be kludged to see if this would work as intended. At this point we had a short discussion about timing and possible MI application for this board. Bob will go away and think about it some more.

The question of replacing the 21062 DSP with a 21060 DSP was addressed. They are pin-for-pin compatible. The 21062 has more memory (4 Mbits compared to 2 Mbits). However, they are not the same family of DSP so some testing should be done with a current board with the DSP replaced before one could verify that this would work. There are no obvious show-stoppers. The larger memory is thought to be useful but not required (gives headroom).

An FPGA could be added to the board, but that makes the project a re-design of the board, not a simple modification of an existing, working, production design. This is thought to add months to the project for the redesign work.

A slight digression to discuss timescales of board modifications, prototyping, ordering, etc. was made at this time. If one assumes that all the testing work has been completed and the final design is in place the timescales look like the following:

1. Order parts (4 weeks)
2. Order circuit boards (2-4 weeks), overlapped with 1.
3. Get approvals for full order (6 weeks, also some overlap)
4. 3 prototypes (2 weeks) + time to verify the functionality.
5. Rest of order (125 boards) (1 month)

Some of the times listed are estimates and aren't usually known until the order is underway. In addition, after the boards are built they need to be tested, etc. after they arrive.

Finally, we talked about the issues involved in obtaining a test stand and how to proceed. We talked about what components are necessary:

- VXI crate
- SLOT 0 board
- VXI UCD board
- DSR board

The possibilities are :

- Setting up a standalone teststand in FCC
- Putting a teststand in A1

- Putting a teststand in Brian Chase's lab area

We decided that a teststand in Brian Chase's area would be best, given the access to experts of the system and ACNET, etc.

The action items for the next meeting are:

1. Work on getting a crate teststand ASAP.
2. Get Echotek block diagram and send it to everyone.
3. Get Echotek quote/timescale once 2) is in hand.

It should be noted that there will be or are Echotek and Damper board setups in A1 for looking at the beam.

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